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(54) Interrupted resonance energy transfer system.

(57) A drive circuit (29) for applying a supply voltage (+V) to a sending coil (10) provides resonant coupling of the sending coil (10) with a target coil (34) regardless of changes in the inductance of the sending coil (10), as long as the resonant frequency of the sending coil (10) is greater than the resonant frequency of the target coil (34). A controller (44) provides variable delay intervals in the application of the supply voltage (+V), thereby compensating for changes in the sending coil's (10) inductance with the passage of time and proximity effects. The controller (44) examines the reflected voltage induced in the sending coil (10) by changing currents in the target coil (34) to examine the degree of resonant coupling between the two coils (10, 34) and correct any mistuning.

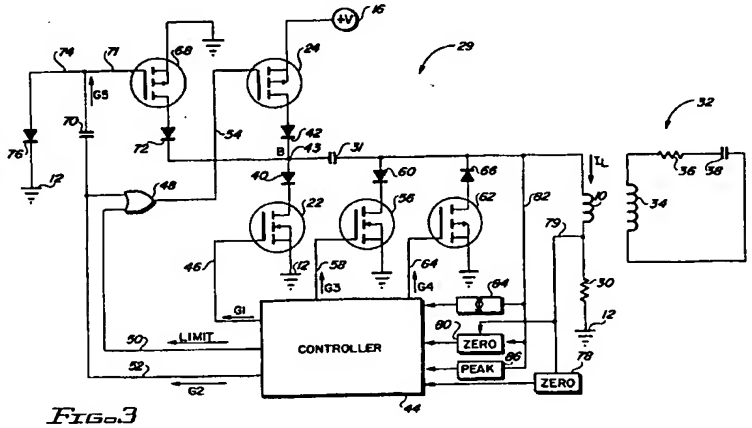

FIG. 3

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Background of the Invention

This invention relates generally to electrical energy transfer circuits and, more particularly, to circuits for driving an inductive element with an applied voltage at a tuned frequency.

It is often necessary to inductively transfer electrical power from one device to another, such as when a charging device is used for recharging a target device's batteries. Each device includes a coil, and the electrical power is inductively transferred from the coil in the charging device typically to the coil in the target device and then to the batteries. To maximize the transfer of energy to the target device's coil, and therefore maximize the rate at which the batteries will be recharged, while also minimizing the energy lost as heat, the coil circuit in the target device typically is tuned by using a capacitor to counteract the reactive impedance of the coil. The coil and capacitor of the target device form an L-C circuit whose impedance will be minimized at the L-C circuit's resonant frequency. Using capacitive tuning to minimize the heat generated by recharging is especially important where the target device will be implanted in a body, such as a heart pacemaker or drug pump, because a rise in the implanted device's temperature of even a few degrees Fahrenheit can cause damage to healthy tissue.

The resonant frequency of the target coil circuit will be determined by the coil inductance, the capacitance, and the physical orientation of the various components and their proximity to other conductors. While the inductance of a coil is largely determined by the size of the coil and the number of coil turns used, the inductance of a coil will be decreased as it is brought into proximity with other conductors. An implanted device, such as a heart pacemaker, is typically contained in a conductive case, and therefore its coil has a relatively stable inductance once encased regardless of any other conductors that are moved nearby. Thus, the resonant frequency of the implanted coil circuit will not appreciably change as the external sending coil of the recharging device is brought close by.

Having fixed the target coil's resonant frequency, maximum inductive coupling is achieved by configuring the recharging device's coil to have the same frequency. That is, the recharging device's coil circuit should generate a field having a fundamental frequency equal to the resonant frequency of the target device's coil circuit. The inductance of the sending coil, and therefore the frequency of its generated field, can change as it is moved close to the case of the target device for recharging. This alters the coupling between the sending coil and the target coil, decreasing the energy transfer and resulting in increased heat generation.

The inductance of a coil can also be changed with the passage of time. Even when new, there is typically a slight variation in the inductance from coil to coil due to manufacturing tolerances. Thus, it is not uncommon to find that the coupling between the sending coil and the target coil is not optimal. This wastes energy, increases the recharging time, and can pose a health risk from heating.

From the discussion above, it should be apparent that there is a need for an energy transfer system for inductively transferring power from an external sending coil to an implanted target coil while maintaining resonant coupling between the coils. The present invention satisfies this need.

Summary of the Invention

The present invention, as defined in the claims, provides an energy transfer system in which the fundamental magnetic field frequency produced by a sending coil circuit with a sending coil and capacitive element can be matched to the resonant frequency of a circuit comprising a target coil and a capacitive element, regardless of variations in the inductance of the sending coil, as long as the resonant frequency of the sending coil circuit is greater than that of the target coil circuit. This increases the coupling of energy from the sending coil to the target coil, maximizing the amount of energy transferred, while still maintaining the coupling of the two coils at the resonant frequency of the target coil circuit, minimizing the amount of energy lost as heat.

The energy transfer system maintains resonant coupling by cyclically transferring energy from a supply voltage source to the sending coil and a capacitor connected in series, thereby producing a cyclic voltage and current. A cyclic drive signal begins the voltage and current cycle for the coil and capacitor, which together comprise an L-C circuit. The sending coil and the capacitor are allowed to go through only one-half of their voltage-current cycle before the cycle is momentarily paused, or maintained at a steady state, at the moment of peak coil current. During this pause, energy is stored in the sending coil. After an appropriate waiting time interval, the second half of the cycle is completed as the coil current decreases to zero and then flows in the opposite direction. The cycle time of the drive signal is a predetermined time interval selected such that the sending coil current frequency is at least as great as the resonant frequency of the target coil circuit. The sending coil current is held at its peak value during the waiting time contained within the predetermined cycle time. In this way, the sending coil is driven resonantly to produce a coil current, and therefore

a magnetic field, having a fundamental frequency equal to the resonant frequency of the target coil circuit and below the natural resonant frequency of the sending coil circuit. The predetermined drive signal cycle time is independent of the resonant frequency of the sending coil circuit, and therefore the predetermined cycle time can be selected to produce a sending coil field having a frequency equal to the resonant frequency of the target coil circuit regardless of minor variations in the sending coil circuit resonant frequency.

In another aspect of the present invention, the operating frequency of the system is adjusted to match the resonant frequency of the target coil circuit despite changes in the resonant frequency of the coil-capacitor circuit over time. For example, if the resonant frequency of the sending system changes as it is brought close to the target device, then the system will adjust the frequency of the produced field such that it is equal to that of the target circuit to maintain resonant coupling. In addition to halting, or pausing, in the cyclic voltage and current of the sending coil circuit, the system adds another pause in the cycle when the sending coil current goes through zero current as it changes direction. When the current of the sending coil reaches zero current, the system disconnects the supply voltage source from the sending coil circuit, placing the circuit in a waiting time interval, and examines the reflected voltage coming from the target device. This waiting time interval comprises a window during which the voltage generated by the reflected power can be checked. Any phase error indicates that the two circuits are not optimally coupled. The cycle time interval can be adjusted until the phase error detected during the window period is substantially zero.

A controller is provided to respond to the differences in system voltage. The windows are used to examine the reflected voltage, while the controller adjusts the delay time to achieve optimum resonant coupling between the devices. In this way, the system compensates for the changing inductance of the sending coil circuit as it is brought close to the target device, and also compensates for changes in the target circuit resonant frequency.

Other features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate by way of example, the principles of the invention.

Brief Description of the Drawings

FIG. 1 is a schematic diagram of a drive circuit in accordance with the present invention.

FIG. 2 is a timing diagram for various waveforms of the drive circuit illustrated in FIG. 1.

FIG. 3 is a schematic diagram of a drive circuit of the type illustrated in FIG. 1, further incorporating a peak controller.

FIG. 4 is a timing diagram for various waveforms of the drive circuit illustrated in FIG. 3.

FIG. 5 is a diagram of various current and voltage waveforms of the drive circuit illustrated in FIG. 3.

Description of the Preferred Embodiment

A resonant energy transfer system in accordance with the present invention is illustrated in FIG. 1, in which a sending coil 10 is used to transfer electrical energy to a target coil 11. For example, the receiving coil can be part of an implanted heart pacemaker having rechargeable batteries. The circuit provides maximum inductive coupling of the two coils 10 and 11 while producing a minimum of heat, thereby reducing the recharging time and decreasing the health risk associated with warming of the pacemaker. The circuit illustrated in FIG. 1 operates such that the frequency of the field produced by the sending coil 10 is equal to the resonant frequency of the target coil 11 circuit.

The sending coil 10 is connected at one end to a reference potential 12, such as ground, via a first diode 14, and to a supply voltage source 16 via a second diode 18. The supply voltage source produces a voltage having a magnitude of +V. One lead of a capacitor 20 is connected between the sending coil 10 and the first diode 14, and the other lead of the capacitor 20 is connected to the reference potential 12. Two transistors, a first transistor 22 and a second transistor 24, alternately connect the coil 10 to the supply voltage source 16 and to the reference potential 12. The first transistor 22 is an n-channel, or NMOS-type transistor, and the second transistor 24 is a p-channel, or PMOS-type transistor. Other transistor types, however, can be used. The gate terminal of each transistor 22, 24 is driven by a voltage from a drive voltage source 26. The drain terminal of each transistor 22, 24 is connected to the sending coil 10 at a junction point 28. The source terminal of the first transistor 22 is connected to the reference potential 12, while the source terminal of the second transistor 24 is connected to the supply voltage source 16. The drive signal produced by the drive voltage source 26 has a predetermined cycle time that is equal to that of the target coil 11 circuit. That is, the frequency of the drive signal is equal to the resonant frequency of the target coil 11 circuit.

The operation of the FIG. 1 circuit is best understood with reference to the timing diagram illustrated in FIG. 2, which illustrates the drive voltage V_A, the voltage V_B of the junction point 28, the

voltage V_C of the capacitor 20, and the current I_L through the sending coil 10. Initially, just before time T1, the drive voltage V_A is high, and therefore the first transistor 22 is in a conducting state, or is biased on, while the second transistor 24 is in a non-conducting state, or is biased off. A negative current has been flowing in the circuit before the time T1, and the capacitor 20 has no energy stored. Thus, the capacitor voltage V_C before time T1 is at zero. At time T1, the drive voltage V_A drops, placing the second transistor in a conducting state, or biasing it on.

Once the drive voltage V_A drops, the voltage V_C on the capacitor 20 is initially at zero. Because the second transistor 24 is conducting at time T1, the opposite lead of the sending coil 10 is at the supply voltage level +V. Thus, at time T1 a positive voltage has been placed across the coil 10, opposing the flow of current I_L. Therefore, the coil current I_L begins changing to an opposite polarity, changing from negative toward positive. The voltage on the first diode 14, however, remains at zero while the diode 14 is conducting, and therefore the capacitor voltage V_C remains at zero. Once the coil current I_L reaches zero, it reverses and becomes positive. The capacitor voltage waveform V_C begins rising in a generally sinusoidal curve toward the supply voltage level +V because the second lead of the sending coil 10 is at that level.

As long as the sending coil current I_L is flowing in the negative direction, the current I_L flows through the first diode 14. When the coil current I_L reaches zero, at time T2, the capacitor voltage V_C that was clamped to ground by the first diode 14 is free because the first diode 14 opens. That is, the first diode 14 cannot conduct current in the opposite (positive) direction. At that time, time T2, the positive current I_L begins charging the capacitor 20. As the voltage V_C across the capacitor 20 increases, the voltage across the coil 10 decreases, and therefore the rate of increase of the coil current I_L decreases. Once the capacitor voltage V_C reaches the supply voltage +V level, the rate of increase for the coil current I_L becomes zero. That is, the coil 10 has a current flowing through it but a zero voltage across it. Thus, the second transistor 24 is biased on, but there is nothing to increase the current I_L through the coil 10. At this point, at time T3, the second diode 18 begins to conduct. Therefore, the coil current I_L stays constant until the transistors 22 and 24 are switched again. The capacitor voltage V_C stays constant because it is clamped to the supply voltage +V by the second diode 18.

The time interval during which the capacitor voltage V_C remains at zero, from time T1 to time T2, is approximately equal to the square root of the inductance multiplied by the capacitance, divided by two. During this interval, the change in inductor current I_L is approximately linear. The time interval during which the capacitor voltage V_C rises toward the supply voltage level +V, from time T2 to time T3, is approximately equal to the constant PI multiplied by the square root of the inductance multiplied by the capacitance, all divided by two. During this time interval, the capacitor voltage V_C waveform has a generally sinusoidal shape, as shown in FIG. 2.

At time T4, the drive voltage V_A again goes high, placing the first transistor 22 in a conducting state and placing the second transistor 24 in a non-conducting state. The voltage supply source 16 is now working against the current I_L flowing through the sending coil 10, which is flowing in the positive direction with the second diode 18 conducting. Because the first transistor 22 is in a conducting state, the current I_L through the sending coil will be in the opposite polarity from the supply voltage +V, proceeding from the first transistor 22, through the sending coil 10, through the second diode 18, and up to the supply voltage source 16. That is, at this point, energy from the coil 10 is being released back into the supply voltage source 16. The sending coil current I_L is decreasing linearly because the supply voltage +V across the coil 10 during this time is not changing and is not charging the capacitor 20. Rather, the voltage is against the flow of current I_L and is decreasing the current I_L. This time interval, from time T4 to T5, is approximately equal to the time interval from time T1 to T2.

When the current I_L through the sending coil 10 reaches zero at time T5, the second diode 18 turns off, and therefore the energy in the capacitor 20 can be transferred into the circuit. The capacitor 20 will transfer its energy into the coil 10 because the first transistor 22 is still conducting current through the ground 12, and therefore, the shape of the waveform from time T5 to T6 will be sinusoidal in the same manner as the waveform from the first half-cycle of the voltage period, from time T2 to T3. Thus, the capacitor voltage V_C begins at a constant level at time T4 and then curves down in a sinusoidal fashion at time T5 until it reaches zero at time T6, the current I_L through the sending coil 10 meanwhile changing linearly from its maximum positive value at time T4, to zero, to its maximum negative value at time T6. The current I_L through the coil 10 becomes more negative from time T4 to T6 because the right hand side of the coil 10 has the supply voltage charge +V from the capacitor 20 initially, and the left hand side has a short to ground 12 through the first transistor 22. When the coil current I_L reaches its peak negative value, the condition of the circuit again corresponds to that just before time T1.

In the circuit illustrated in FIG. 1, the sending

coil 10 and capacitor 20 are selected so as to comprise an L-C circuit having a resonant frequency at least as high as that of the target coil 11 circuit. The half-cycle time of the drive voltage V_A can be selected to be approximately equal to half the cycle time for the resonant frequency of the target coil 11 circuit. As can be seen in FIG. 2, the half-cycle time of the voltage V_C and current I_L in the sending circuit is independent of the resonant frequency of the circuit. Thus, the time interval from time T1 to time T4 can be predetermined to match the half-cycle time of the target coil 11 resonant frequency regardless of changes in the sending coil 10 inductance, as long as the resonant frequency of the circuit is above that of the target coil circuit. In this way, the cyclic voltage V_C and current I_L in the sending coil 10 circuit will be in resonance with the target coil 11 circuit. That is, the waiting time interval from time T3 to time T4 and from time T6 to time T7 will each be a waiting time interval to ensure resonant coupling between the two coils.

In another embodiment of the invention, shown in FIG. 3, a second waiting time interval is added. The first waiting time interval described above with respect to FIGS. 1 and 2 ensures resonant coupling between the two coils 10 and 11 despite changes in the sending coil's 10 inductance, because the waiting time interval contained within the drive signal cycle time can accommodate changes while the cycle time remains fixed, and allows energy to be stored in the coil 10. The embodiment illustrated in FIG. 3 also includes a first waiting time interval during which energy is stored, and also includes a second waiting time interval. The added second waiting time interval is used as a window during which the very small reflected voltage induced in the sending coil by the target coil is examined. This allows precise determination of the degree of matching between the two circuits. If the voltage waveform indicates that resonant coupling has been lost, the first waiting time interval can be adjusted until the waveform indicates that resonant coupling is achieved. A drive circuit 29 is shown in FIG. 3 in which, as with the previous embodiment of FIG. 1, the sending coil 10 is alternately connected either to a reference potential 12, such as ground, or to a supply voltage source 16 via a first transistor 22 or a second transistor 24, respectively. The sending coil 10 is connected to ground via a sensing resistor 30. A capacitor 31 is connected in series to the coil 10, and the two comprise an L-C circuit having a resonant frequency and producing a cyclic voltage and current flow. The cyclic voltage and current are produced in conjunction with the first waiting time interval, or delay, that can be tuned such that the voltage and current cycles have a frequency substantially equal to the resonant frequency of a target device 32 having a target coil 34 connected in series with a resistor 36 and a capacitor 38. That is, in the FIG. 3 circuit the delay interval is again used to match the half-cycle time of the cyclic voltage and current of the drive circuit 29 to the half-cycle time of the resonant frequency of the target device 32. The added second waiting time interval, or window, is used to disconnect the sending coil 10 from the first and second transistors 22 and 24 and to allow the very small reflected voltage from the target coil 34 to be compared to the voltage of the sending coil 10. A phase error in the reflected voltage indicates that the two coils 10 and 34 are not resonantly coupled. There can be a phase shift in the target voltage waveform from what would otherwise be expected due to an intervening conductor, such as the pacemaker case as noted above, and therefore a phase error will not necessarily be present whenever there is a phase difference. Therefore, the particular configuration of the system will determine the amount of phase difference expected and therefore the presence of a phase error.

The two transistors 22 and 24 advantageously comprise MOSFET-type transistors of opposite polarity, the first transistor 22 being an n-channel MOSFET and the second transistor 24 being a p-channel MOSFET. The drain terminals of the first and second transistors 22 and 24 are connected to the capacitor 31 by first and second diodes 40 and 42, respectively. The diodes 40 and 42 are connected at a common junction point 43 labeled B. The source terminal of the second transistor 24 is connected to the voltage supply source 16. The source terminal of the first transistor 22 is connected to the reference potential 12, or ground.

A controller 44 controls the alternating connection of the sending coil 10 with the supply voltage source 16 and the reference voltage 12. The controller 44 includes a variable oscillator and a pulse generator for producing the various drive signals. The controller 44 is connected to the first transistor 22 via a line 46 over which the controller 44 sends a drive signal G1. When the drive signal G1 is high, the first transistor 22 is placed in a conducting state, or is biased on, thereby connecting the junction 43 to the reference potential 12 or a negative voltage. The controller 44 is connected to the gate terminal of the second transistor 24 through an OR-gate 48. One lead of the OR-gate 48 is connected to the controller 44 via a line 50 over which the controller 44 sends a LIMIT signal indicating that a desired voltage limit has been reached. The second lead of the OR-gate 48 is connected to the controller 44 via a line 52 over which the controller 44 sends a drive signal G2. The OR-gate, in turn, is connected to the gate

terminal of the second transistor 24 via a line 54. If either the LIMIT signal or the G2 driving signal is high, the second transistor 24 is placed in a non-conducting state, or is biased off.

Two additional transistors are provided in the circuit 29 for performing a shorting function, as will be described in more detail below. The controller 44 is connected to the gate terminal of a third transistor 56 via a line 58 over which the controller 44 sends a drive signal G3. The third transistor 56 is connected between the sending coil 10 and the capacitor 31 at its drain terminal via a third diode 60. The controller 44 is connected to the gate terminal of a fourth transistor 62 via a line 64, over which the controller 44 sends a drive signal G4, and is connected between the coil 10 and the capacitor 31 at its drain terminal via a fourth diode 66. The third transistor 56 is preferably an n-channel transistor, while the fourth transistor 62 is preferably a p-channel transistor. The third and fourth transistors 56 and 62 periodically short the sending coil 10 to ground to allow the current I_L to idle, as described in more detail below.

A fifth transistor 68 is provided for control of the maximum output voltage produced by the circuit 29. A gate terminal of the fifth transistor 68 receives a control signal G5 comprising the G2 drive signal from the controller 44 received via the line 52 and connected to the fifth transistor 68 through a coupling capacitor 70 via a line 71. The coupling capacitor 70 shifts the voltage level of the G2 signal, thereby creating the G5 signal. That is, the G2 signal varies from the supply voltage +V to the reference potential zero, while the G5 signal varies from the reference potential to negative supply, -V. The fifth 68 transistor is preferably of the same polarity as the second transistor 24. Thus, when the drive signal G2 is high, the fifth transistor 68 is placed in a non-conducting state, or is biased off. The drain terminal of the fifth transistor 68 is connected to the common junction point 43 via a fifth diode 72. The coupling capacitor 70 and gate terminal of the fifth transistor 68 are also connected to ground 12 via a line 74 and a sixth diode 76.

The controller 44 receives input signals from zero crossing detectors 78, 80 and a phase detector 84. A first zero crossing detector 78 provides its output to the controller 44 and is connected at its input between the sending coil 10 and the sensing resistor 30 via a line 79. A second zero crossing detector 80 provides its output to the controller 44, and is provided with a first input from a line 82 connected between the coil 10 and the capacitor 31 and a second input from the line 79. The phase detector 84 provides its output to the controller 44, and is connected at its input between the coil 10 and the capacitor 31 by the line 82. Finally, a peak detector 86 provides its output to the controller 44, and is connected to the drive circuit 29 via the line 82 between the coil 10 and capacitor 31. The peak detector 86 limits the magnitude of the voltage and current produced by the circuit 29.

The operation of the drive circuit 29 is best understood with reference to the timing diagrams of FIG. 4, which illustrate the cyclic drive control signal G1 for the first transistor 22, the cyclic drive signal G2 for the second transistor 24, the drive signal G3 for the third transistor 56, the drive signal G4 for the fourth transistor 62, the drive signal G5 for the fifth transistor 68, the voltage V_B of the junction point 43, the current I_L and voltage V_L of the sending coil 10, and the limit signal applied to the OR-gate 48. FIG. 5 shows the voltage V_R, which is the reflected voltage induced in the drive circuit 29 by the target coil 34, and also the voltage V_T and current I_T of the target coil 34.

The timing diagrams of FIG. 4 show that, initially at time T1, both G1 and G2 are high and therefore the first transistor 22 is biased on and the second transistor 24 is biased off. Thus, the junction point 43 is connected to ground and the junction voltage V_B is at zero. Due to the operation of the circuit before time T1, a decreasingly negative current I_L is flowing through the sending coil 10, the capacitor 31, the first diode 40, the first transistor 22, through ground, back through the sensing resistor 30, and back to the coil 10. Therefore, the coil 10 has an increasingly positive voltage V_L. At time T2, the coil current I_L has reached zero and the coil voltage V_L has reached its maximum value, +V. At this time, a window time interval will be triggered by appropriate operation of drive signals, as explained further below.

Initially, at time T1, all the transistors 24, 56, 62 and 68 except for the first transistor 22 were biased off. When the sending coil current I_L reaches zero at time T2, the first zero crossing detector 78 senses the condition and provides an appropriate signal to the controller 44. The controller 44, in response, begins the window time interval by dropping the drive voltage G1, biasing off the first transistor 22. Therefore, at time T2 all of the transistors 22, 24, 56, 62 and 68 are biased off. With all of the transistors biased off, the terminal of the sending coil 10 closest to the transistors sees the transistors as open switches and "floats," and therefore allows the very small reflected voltage V_R induced in the sending coil 10 by the changing currents in the target coil 34 to be seen by the phase detector 84, which is connected between the coil 10 and the capacitor 31. The controller 44 makes use of the reflected voltage V_R to adjust the operation of the drive circuit 29, as described further below in conjunction with FIG. 5.

At time T3, after a predetermined time interval, the controller 44 ends the window time interval by

dropping the drive voltage G2 for the second transistor 24, biasing on the second transistor 24. Thus, the junction point 43 is connected to the supply voltage source 16 and the voltage V_L on the sending coil 10 jumps to +V. Beginning at time T3, the coil current I_L rises in a sinusoidal fashion for a quarter cycle as the voltage across the capacitor 31 rises, thereby decreasing the voltage V_L on the coil 10. At time T4, the coil current I_L reaches a peak while the voltage across the coil V_L reaches zero. That is, all of the voltage from the supply voltage source 16 is across the capacitor 31. The second zero crossing detector 80 is triggered at time T4 by the zero voltage across the coil 10 to begin a delay time interval. The detector 80 is provided with both the coil voltage V_L and the voltage across the resistor 30 to more precisely react at the zero coil voltage. While the voltage across the resistor 30 will be very small, those skilled in the art will appreciate that providing this voltage to the zero crossing detector 80 allows the resistor voltage to be subtracted from the coil voltage V_L, eliminating it from the total and thereby allowing the zero crossing detector 80 to respond when the coil voltage V_L itself truly crosses zero.

At time T4, the controller 44 receives the signal from the second zero crossing detector 80 and begins a delay time interval by dropping the drive voltage G4, biasing on the fourth transistor 62 and producing a low resistance path for current in the positive direction through the fourth transistor 62 and the fourth diode 66 to the sending coil 10, to allow the current I_L in the sending coil 10 to continue circulating. The controller 44 varies the delay interval to make the drive frequency of the circuit 29 match the resonant frequency of the target system 32 as described below. It should be noted that, although the third transistor 56 is shown as being biased off during this delay time, both the third transistor 56 and fourth transistor 62 could be biased on at the same time, because the current would still flow only through the fourth transistor 62 and fourth diode 66. The level of the coil current I_L from time T4 to T5 is shown as slightly decreasing to illustrate that various losses in the circuit will slightly decrease the produced current. These losses include diode losses, coupling inefficiencies, and inductance losses. During the delay time interval, the second transistor 24 has been biased on, but no current was flowing because the right side of the capacitor 31 was held at zero voltage by the fourth transistor 62.

At time T5, the controller 44 ends the delay by biasing off the fourth transistor 62. The resonant energy transfer is continued for another quarter cycle as energy in the sending coil 10 is transferred to the capacitor 31 from time T5 to T6, as illustrated by the sinusoidal decrease in voltage and current for the coil 10. Therefore, at time T6 the voltage of the junction point 43 can rise above the level of the supply voltage source. When the current I_L of the sending coil 10 has dropped to zero at time T6, the voltage across the sensing resistor 30 goes to zero, thereby triggering the first zero crossing detector 78 and resulting in the controller 44 initiating the next window time interval.

During the window time interval beginning at time T6, all of the transistors 22, 24, 56, 62, 68 are again biased off by the controller 44. The terminal of the sending coil 10 closest to the capacitor 31 "floats" and allows the phase detector 84 to see the voltage induced in the sending coil 10 by the changing current in the target coil 34. The phase detector 84 provides an appropriate signal to the controller 44, which can adjust the delay time interval so as to match the operating frequency of the target coil.

When the controller 44 wants to end the window time interval at time T7, the controller 44 raises the G1 drive signal, thereby biasing on the first transistor 22. When the first transistor 22 is biased on, a current can flow from the first transistor 22, through ground, through the sensing resistor 30, the sending coil 10, the capacitor 31, and the first diode 40. Therefore, the capacitor 31 can release the energy that had been stored in it, which was at greater than the supply voltage +V. Therefore, the voltage V_L across the coil 10 can be greater than -V, as shown in FIG. 4. The circuit can continue to operate in this way, swinging above the supply voltage, limited by the quality factor Q of the circuit, as described below. When the capacitor voltage has reached zero, all of the energy from the capacitor 31 has been released into the circuit and the coil voltage V_L will be at zero, as shown in the timing diagram at time T8.

At time T8, the current I_L is flowing in the negative direction, and therefore the third transistor 56 will be used to short the sending coil 10 rather than the fourth transistor 62 used previously. Therefore, the controller 44 triggers another delay time interval by raising the drive signal G3, biasing on the third transistor 56. The current I_L will continue to circulate from the coil 10 through the third diode 60 and the third transistor 56 back to the coil 10 while the delay lasts. At time T9 the controller 44 will drop the G3 drive signal, biasing the third transistor 56 off, and energy will transfer from the inductor 10 back into the capacitor 31 with an opposite polarity. That is, the current I_L will be decreasingly negative, moving toward the positive. When the current I_L reaches zero at time T10, the first zero crossing detector 78 senses the condition and provides an appropriate signal to the controller 44. The controller 44 in response begins the window interval by dropping the G1 drive signal, bias-

ing the first transistor 22 off. Thus, it can be seen that window time intervals are achieved by biasing off all of the transistors 22, 24, 56, 62, 68, while delay time intervals are achieved by shorting the sending coil 10 to the ground 12.

FIG. 5 shows the waveforms for the drive and reflected voltages V_L and V_R, respectively, drawn as solid lines where the drive frequency of the sending coil circuit 29 matches the resonant frequency of the target coil circuit 32, and shows the waveforms as a dashed line where the driving frequency is too high. The total voltage across the sending coil 10 is shown in FIG. 5 as the voltage $V_L + V_R$, or the sum of the driving voltage and the reflected voltage V_R. That is, the coil voltage V_L is the voltage caused by the drive circuitry 29 and is what would be seen if no receiving circuit 32 was inductively coupled, and the reflected voltage V_R isthe voltage induced in the sending coil 10 by the changing currents in the target coil circuit 32. Although always present, the reflected voltage V_R is not readily observable unless all of the transistors 22, 24, 56, 62, 68 are biased off. Unlike the V_L waveform illustrated in FIG.4, the V_L waveform of FIG. 5 is shown in an idealized form, having fluctuations in the voltage level that are symmetric about zero. This is done for purposes of simplicity in viewing the combined V_L+V_R voltage waveforms.

The circuit illustrated in FIG. 3 will transfer energy with each cycle, building up the energy transferred between the sending coil 10 and the capacitor 31 as described above until the voltage at the junction 43 will swing well beyond the supply voltage and ground. The peak value will be limited by a circuit characteristic known as the quality factor Q, known to those skilled in the art. The peak voltage ultimately reached at the junction will be $2Q^{*}(+V)/\pi$. While switching losses, diode voltage drops, and loading from the target circuit 32 will add to the losses, the ultimate peak reached could still be a very large number. The fifth transistor 68 and the LIMIT signal produced by the controller 44 control the amplitude reached, connecting the sending coil 10 and capacitor 31 with ground 12 instead of the supply voltage source 16.

The interaction of the second transistor 24, the fifth transistor 68, the controller 44, and the losses described above are illustrated in the FIG. 4 timing diagram for the voltage V_L of the sending coil 10 and the drive signals produced by the controller 44. At time T17, for example, the coil voltage V_L is rising and reaches its peak at time T18 when the coil current I_L reaches zero. Just before time T18, however, the coil voltage V_L reaches a value greater than a predetermined maximum and triggers an output from the peak detector 86 to the controller 44. Other suitable signaling mechanisms can be used, however, such as maximum coil current or magnetic field strength.

When the coil voltage V_L exceeds the predetermined maximum, just prior to time T18, the controller 44 produces the LIMIT signal to bias off the second transistor 24. Thus, at time T19, when the signal G2 drops to bias on the second transistor 24 and fifth transistor 68, the operation of the OR-gate 48 with the LIMIT signal biases the second transistor 24 off, while the fifth transistor 68 is left biased on. Therefore, a current can continue to flow through the capacitor 31, the sending coil 10, the sensing resistor 30, through ground, through the fifth transistor 68, and the fifth diode 72. This prevents the coil voltage V_L and the current I_L from increasing to levels greater than the desired peak. The diagram in FIG. 4 also shows that when the coil voltage V_L decreases below the desired maximum, such as at time T25, the LIMIT signal is again dropped, thus allowing the second transistor 24 to again be biased on and off with the signal G2 as with the usual operation of the circuit described above.

If the target coil 34 is near a relatively large amount of metal, such as where the target coil 34 is located within a metal pacemaker case, the metal will introduce a phase shift in the reflected voltage V_R in addition to the shifts caused by any inductance changes and resulting mistuning from age, physical orientation, and so forth. Those skilled in the art will appreciate that this can be taken into account when designing the phase detector 84. For example, in the case of extremely large phase shifts, or where the phase shift is variable, the drive signals can be stopped for one or more cycles rather than for a narrow window or delay period. This can be done periodically with a suitably low duty cycle, and allows a frequency detector circuit to be substituted for the phase detector shown.

Reference list

10	sending coil
11	target coil
12	reference potential
14	first diode
16	supply voltage source
18	second diode
20	capacitor
22,24	transistors
26	drive voltage source
28	junction point B
29	drive circuit
30	sensing resistor
31	capacitor
32	target device
34	target coil

36	resistor
38	capacitor
40,42	diodes
43	junction point B
44	controller
46	line
48	OR-gate
50,52,54	lines
56	third transistor
58	line
60	third diode
62	fourth transistor
64	line
66	fourth diode
68	fifth transistor
70	coupling capacitor
71	line
72	fifth diode
74	line
76	sixth diode
78	first zero crossing detector
79	line
80	second zero crossing detector
82	line
84	phase detector
86	peak detector
G1 - G5	drive signals
I_L	current through 10
I_T	current through 34
+V	supply voltage level
V_A	drive voltage from 26
V_B	voltage at 28, 43
V_C	voltage across 20
V_L	coil 10 voltage
V_R	reflected voltage induced in 29 by 34
V_T	voltage across 34

Claims

1. A drive circuit, for inductively driving a target coil (11; 34) connected to a first capacitive element (38) and thereby forming a target L-C circuit (32) having a resonant frequency, comprising:

   a supply voltage source (16);

   a sending coil (10) connected to a second capacitive element (20; 31) such that the two form an L-C circuit having a resonant frequency greater than that of the target L-C circuit (32) and being driven by the supply voltage; and

   control means for periodically connecting the supply voltage source (16) to the sending coil (10), such that the supply voltage drives the sending coil (10) to produce a cyclic voltage (V_L) and a cyclic current (I_L) flows through the sending coil (10) circuit, and for disconnecting the supply voltage source (16) from the sending coil (10) and connecting the sending coil (10) to a reference potential (12) after a time interval approximately equal to one-half the resonant cycle time of the target L-C circuit (32);

   wherein the cyclic voltage (V_L) induced in the sending coil (10) is controlled by the control means to be at substantially the same frequency as the resonant frequency of the target L-C circuit (32).

2. A drive circuit as recited in claim 1, wherein the second capacitive element (20) is connected to a first terminal of the sending coil (10) thereby arranged in series with the sending coil (10) between the second terminal (28) of the sending coil (10) and the reference potential (12);

   wherein the control means comprises first and second switching means (22, 24) for controllably connecting the second terminal (28) of the sending coil (10) either to the reference potential (12) or the supply voltage source (16), a first and a second diode (14, 18) connecting the first terminal of the sending coil (10) to the reference potential (12) and the supply voltage source (16), respectively, and drive means (26) producing a cyclic drive voltage (V_A) at a predetermined frequency and connected to control terminals of said switching means (22, 24) thereby controlling said switching means (22, 24) such that the first switching means (22) is in a conducting state when the second switching means (24) is not and vice versa (fig 1).

3. A drive circuit as recited in claim 1, wherein the second capacitive element (31) is connected to a first terminal of the sending coil (10) thereby arranged in series with the sending coil (10) between a junction point (43) and the reference potential (12),

   wherein the control means comprises first and second switching means (22, 24) for controllably connecting the junction point (43) either to the reference potential (12) or to the supply voltage source (16), at least one third switching means (56 or 62) for controllably connecting the first terminal of the sending coil (10) to the reference potential (12) and drive signal means (44) connected to control the terminals of said switching means (22, 24 and 56 or 62) (fig 3).

4. A drive circuit as recited in claim 3, wherein the control means further comprises zero crossing means (80) for detecting when the

produced sending coil voltage (V_L) reaches zero and for producing a delay time interval (T4 - T5, T8 - T9) in response at which the at least one third switching means (56 or 62) is switched on.

5. A drive circuit as recited in claim 4, wherein the control means further comprises phase detector means (84) for detecting phase difference between the sending coil voltage (V_L) and a reflected voltage (V_R) induced in the sending coil (10) from changing currents in the target coil (34) and for adjusting the delay time interval (T4 - T5, T8 - T9) so as to match the operating frequency of the target coil (34).

6. A drive circuit as recited in claim 5, wherein the control means comprises a further zero crossing detector means (78) for detecting when the produced sending coil current (I_L) reaches zero and for producing a window time interval (T2 - T3, T6 - T7) in response at which each of the switching means (22, 24 and 56 or 62) is switched off, whereby the phase difference between the sending coil voltage (V_L) and the reflected voltage (V_R) is detected during this window time interval (T2 - T3, T6 -T7).

7. A drive circuit as recited in one of the claims 3 - 6, wherein the control means further comprises additional controllable switching means (68) coupled between the junction point (43) and the reference potential (12) and peak responding means (86) for responding to a predetermined voltage level in the drive circuit (29) to turn off the second switching means (24) and instead turn on the additional switching means (68).

8. A drive circuit as recited in one of the claims 2 - 7, wherein said switching means (22, 24, 56, 62, 68) are MOS-type transistors.

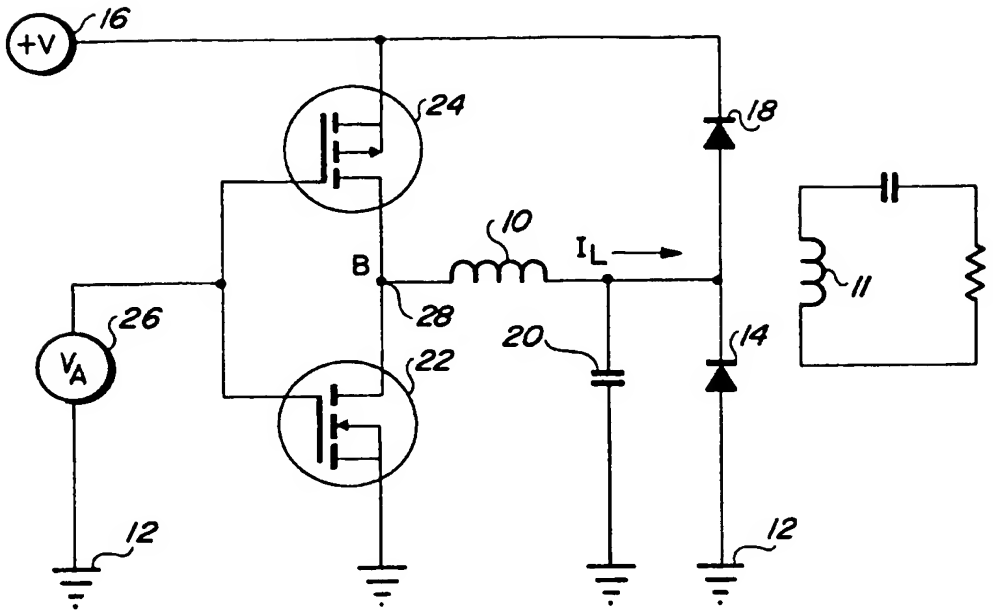

+V
16
24
18
10
I_L
B
11
26
V_A
28
22
20
14
12
12

FIG. 1

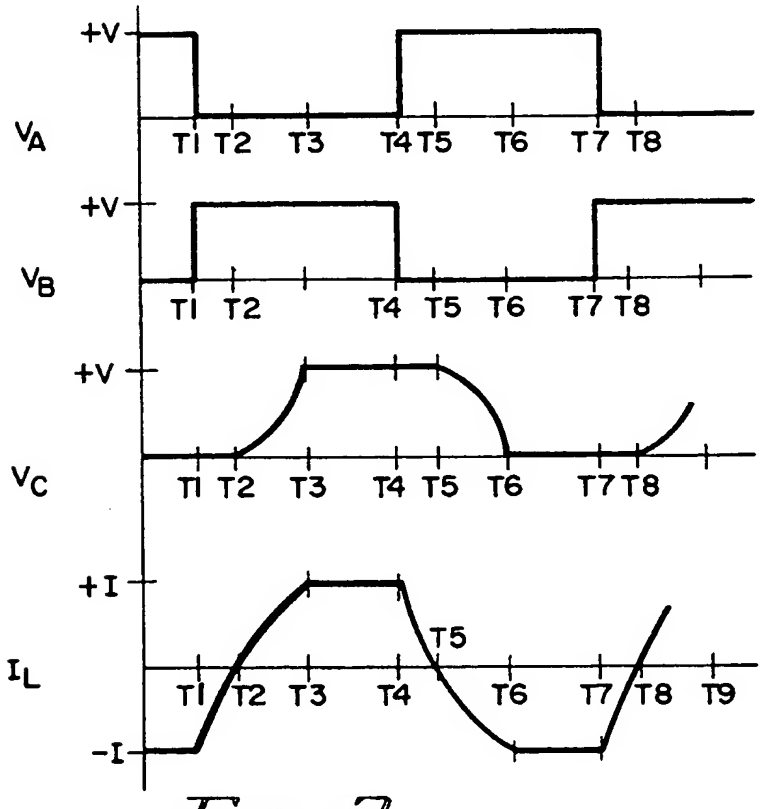

+V
V_A
T1 T2 T3 T4 T5 T6 T7 T8
+V
V_B
T1 T2 T4 T5 T6 T7 T8
+V
V_C
T1 T2 T3 T4 T5 T6 T7 T8
+I
I_L
T5
T1 T2 T3 T4 T6 T7 T8 T9
-I

FIG. 2

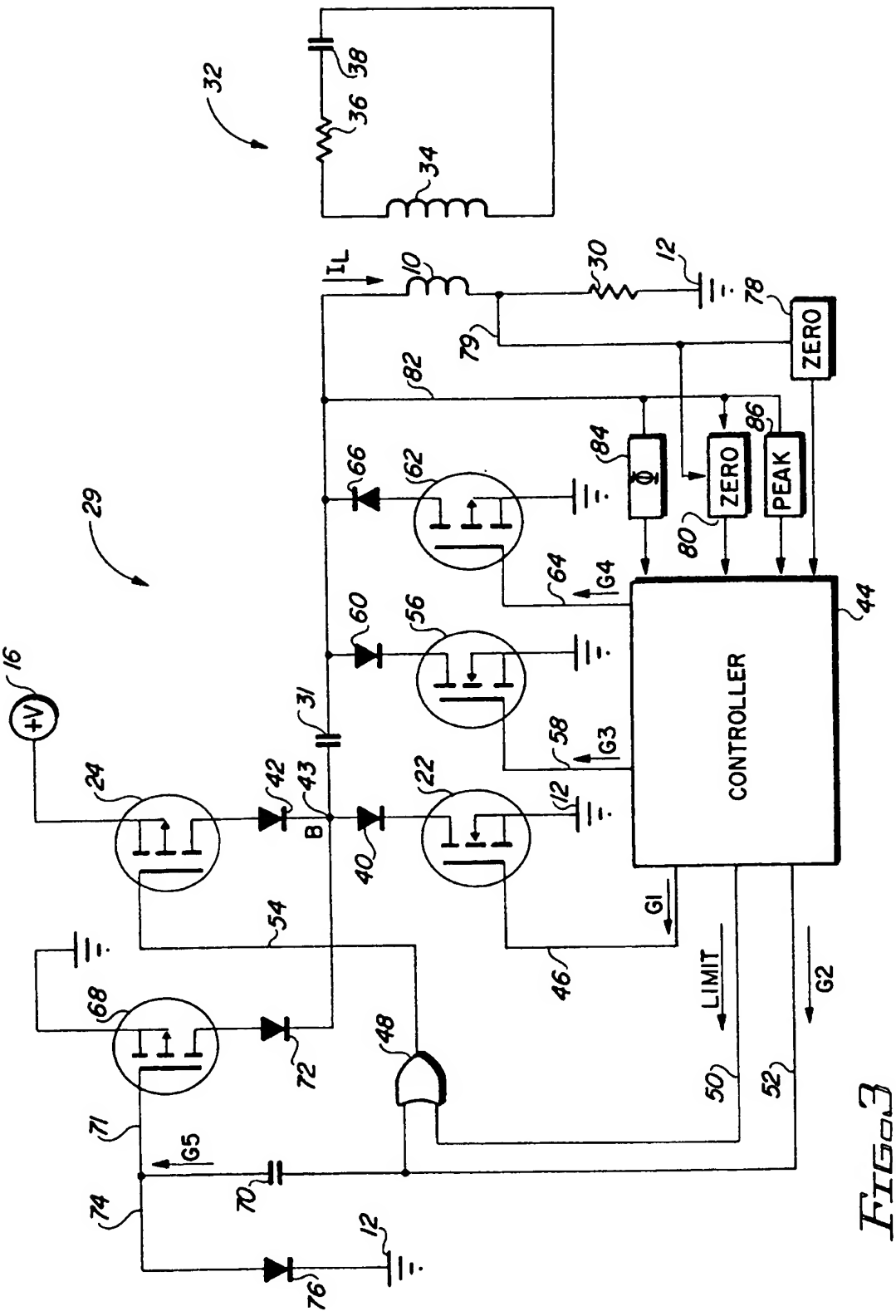
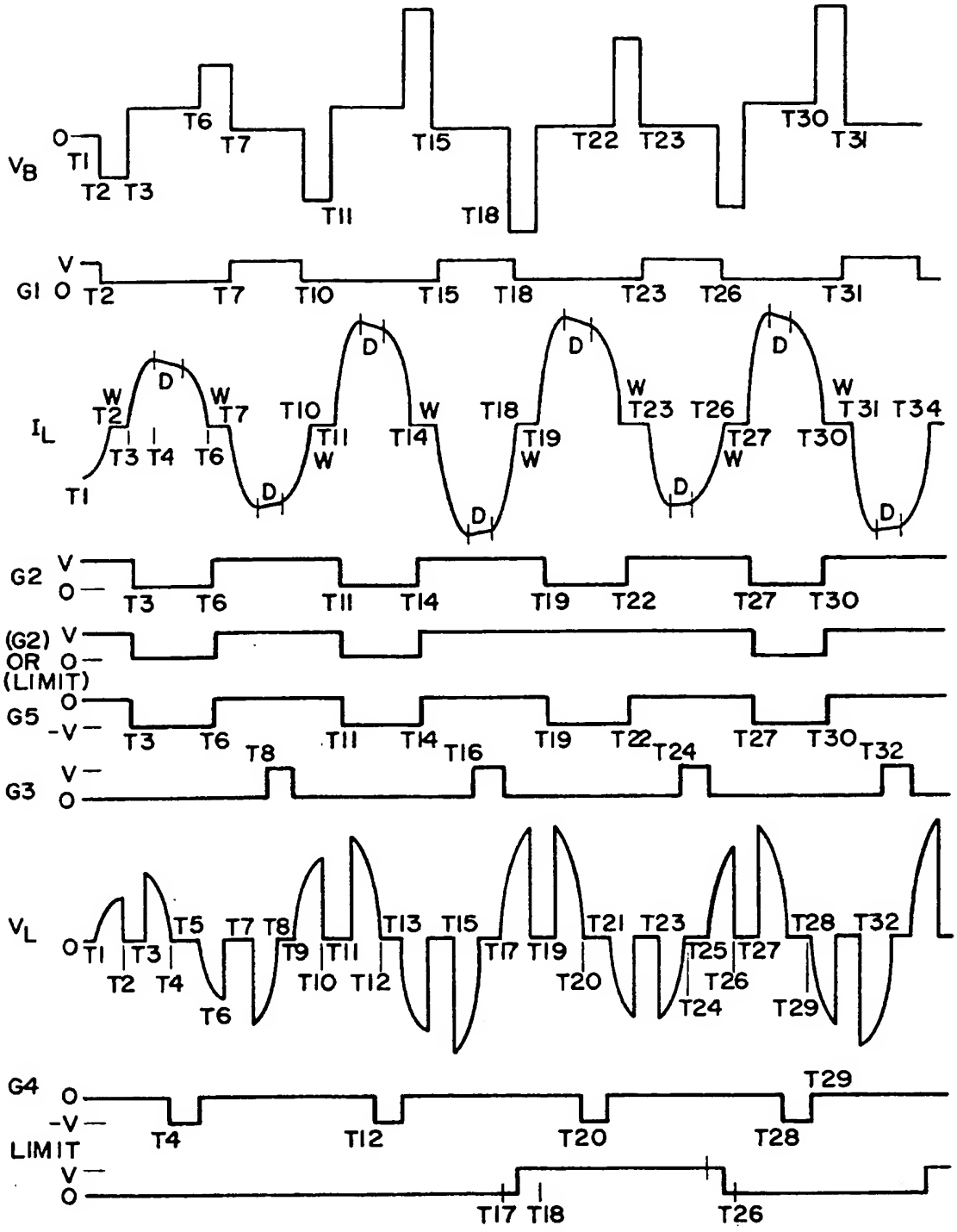

32
38
36
34
IL
10
30
12
78
ZERO
79
82
84
66
62
Φ
ZERO
PEAK
86
80
29
64
G4
60
56
44
CONTROLLER
16
+V
31
58
G3
24
42
43
B
22
12
40
54
G1
46
LIMIT
G2
68
72
48
50
52
71
G5
70
74
12
76

Fig. 3


V_B
O
T1
T2 T3
T6
T7
T11
T15
T18
T22 T23
T30
T31
G1
V
O
T2
T7
T10
T15
T18
T23
T26
T31
I_L
W
D
T1
T2
T3 T4
T6
T7
T10
T11
T14
T18
T19
T23
T26
T27
T30
T31 T34
G2
T3
T6
T11
T14
T19
T22
T27
T30
(G2) OR (LIMIT)
G5
-V
T3
T6
T8
T11
T14
T16
T19
T22
T24
T27
T30
T32
G3
V_L
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T15
T17
T19
T20
T21
T23
T24
T25
T26
T27
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T32
G4
T4
T12
T20
T28
T29
LIMIT
T17 T18
T26

FIG.4

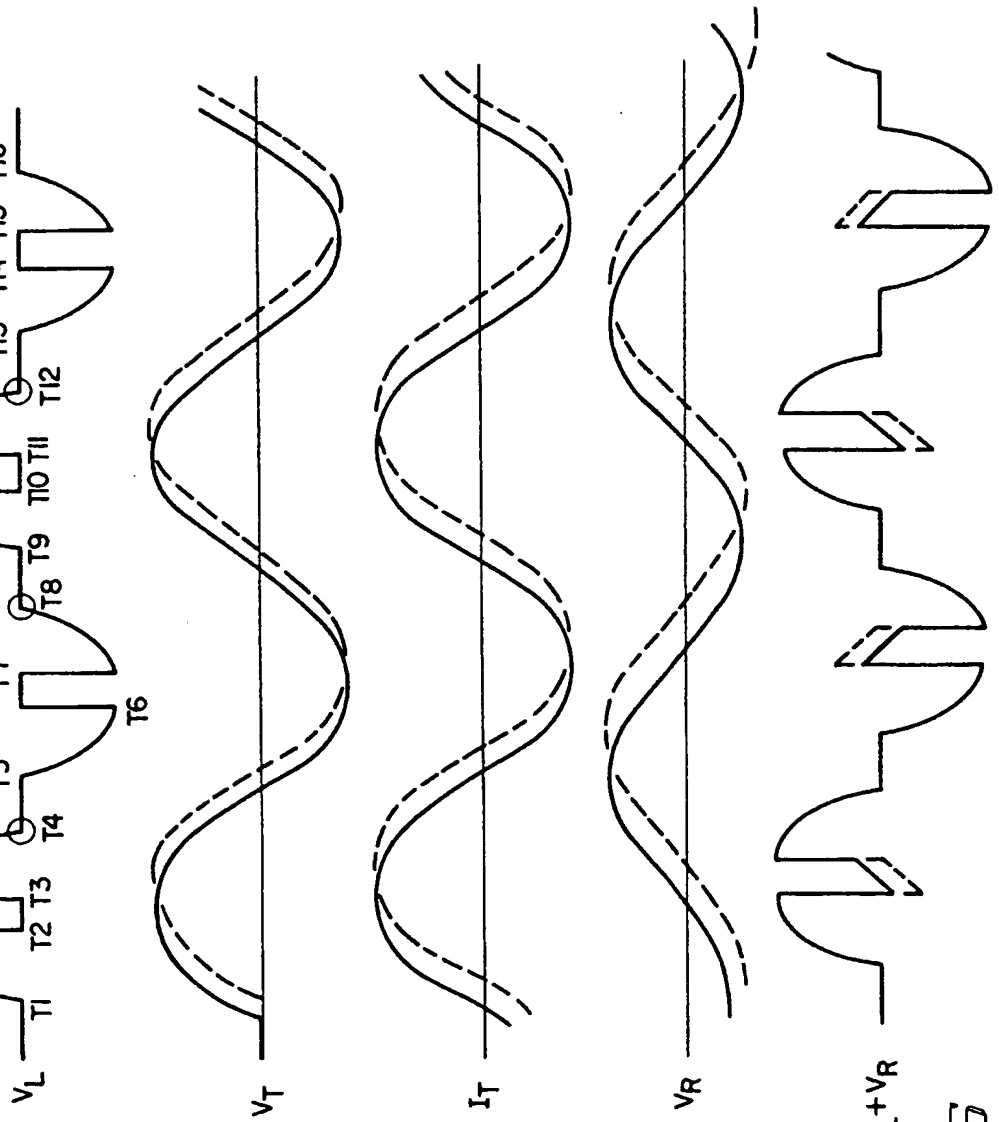
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
V_L
V_T
I_T
V_R
V_L+V_R

Fig.5